REMARKS/ARGUMENTS

In the Office action dated July 30, 2004, the Examiner allowed claims 22 and 23, indicated claims 5, 7-10, 16 and 18-21 to be allowable if rewritten in independent form and continued to reject all remaining claims (claims 1-4, 6, 11-15 and 17) as obvious over Tran in view of Nair. The undersigned had a telephonic interview with the Examiner on October 26, 2004 to discuss the rejected claims. Applicants' arguments were explained to the Examiner. The Examiner requested the Applicants to determine whether a sufficient functional connection existed between data cache and branch prediction arrays to permit the Examiner to use Tran's teachings regarding data cache against the claimed branch prediction array limitations. This and other issues are addressed below. Based on the following arguments and previous arguments submitted to the Examiner, Applicants respectfully submit that all pending claims are patentable over the art of record. To the extent that the Examiner continues to reject the claims, Applicants respectfully request a telephonic interview with the Examiner.

Claim 1 recites that the processor's branch predictor comprises a "multi-bank prediction array that is used for predictions for conditional branch instructions." Further, claim 1 requires bank control logic "to ensure that two accesses to said prediction array in the same cycle do not conflict." The Examiner observes that Tran discloses a branch predictor 220 and a branch prediction array 255 (Fig. 2). Claim 1 requires the conditional branch prediction array to be "multi-bank prediction array." Nowhere in Tran do Applicants find that Tran teaches that the branch prediction array 255 is a multi-bank prediction array. As such, Tran does not appear to be able to support multiple branch instruction predictions being obtained in the same cycle and thus Tran does address the problem solved by the invention of claim 1, that is, how to avoid conflicts when two conditional branch instructions would otherwise target the same bank in a single-ported, multi-bank conditional branch instruction prediction array. The invention of claim 1 solves that problem by including bank control logic "to ensure that two accesses to said prediction array in the same cycle do not conflict." The Nair reference is deficient in this regard.

For the limitation regarding the control logic that ensures that two accesses to the conditional branch prediction array do not conflict, the Examiner turns to columns 189 and 190 of Tran. As the subheading clearly indicates at col. 189, line 43 ("DCACHE"), those columns of Tran discuss data cache, not conditional branch prediction logic of Tran. During the October 26, 2004 telephonic interview, the Examiner requested Applicants to address the issue of whether data cache is functionally similar enough to conditional branch prediction logic and branch prediction arrays to permit the Examiner to use Tran's teachings of data cache with regard to the control logic limitations of claim 1 relating to ensuring "that two accesses to said [conditional branch] prediction array in the same cycle do not conflict." Applicants do not believe there to be any logical connection between data caches and conditional branch prediction logic and arrays. That being the case, Tran's discussion of data cache appears to be generally irrelevant to the subject matter of claim 1. Moreover, columns 189-190 of Tran do not teach or even suggest any logic that prevents conflicts between two accesses in the same cycle to a conditional branch prediction array. Nair is also deficient in this regard.

For either or both of these reasons, claim 1 and all claims that depend from claim 1 are allowable.

The preceding arguments apply to claim 12 as well. The art of record does not teach or suggest a "multi-bank" branch prediction array or "bank control logic...to ensure that two branch prediction accesses to said prediction array in the same cycle do not conflict." Accordingly, claim 12 and dependent claims 13-21 are allowable at least for that reason.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including

fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

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